N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	100V
I_D	60A
$R_{DS(ON)}$(at V_{GS}=10V)	8.6 mohm

100% EAS Tested

100% V_{DS} Tested

General Description

Split gate trench MOSFET technology

Excellent package for heat dissipation

High density cell design for low $R_{DS(ON)}$

Moisture Sensitivity Level 1

Epoxy Meets UL 94 V-

Typical Performance Characteristics

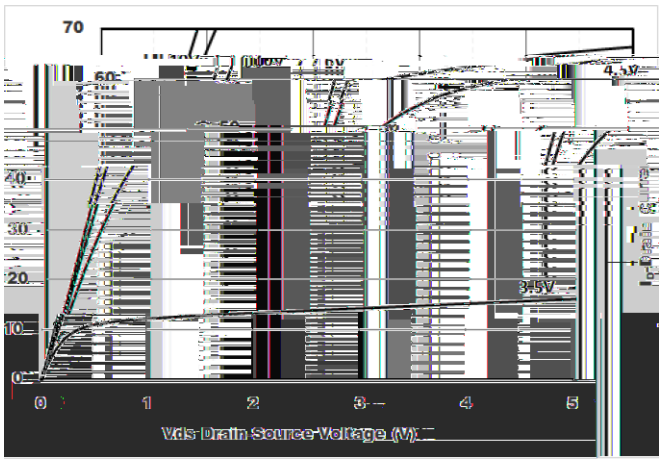


Figure1. Output Characteristics

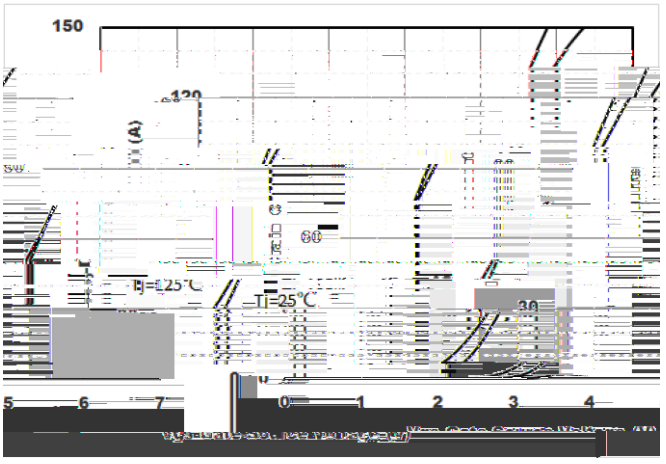


Figure2. Transfer Characteristics

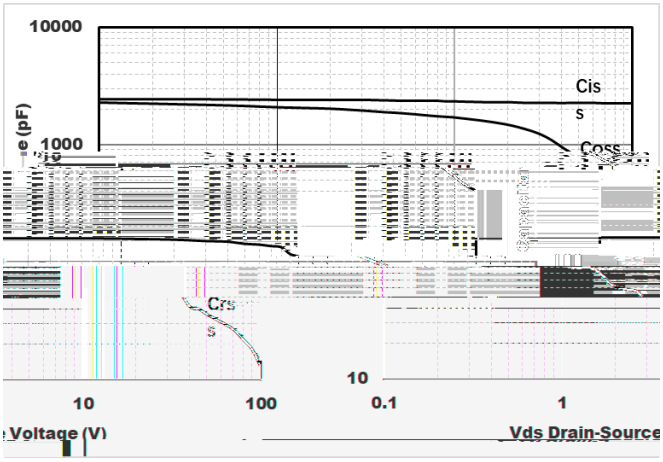


Figure3. Capacitance Characteristics

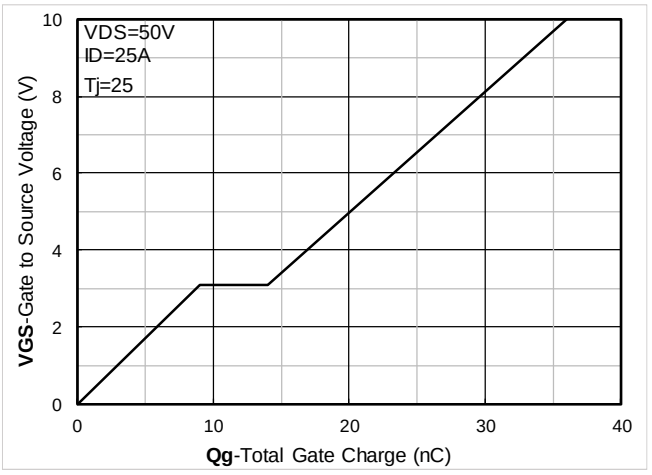


Figure4. Gate Charge

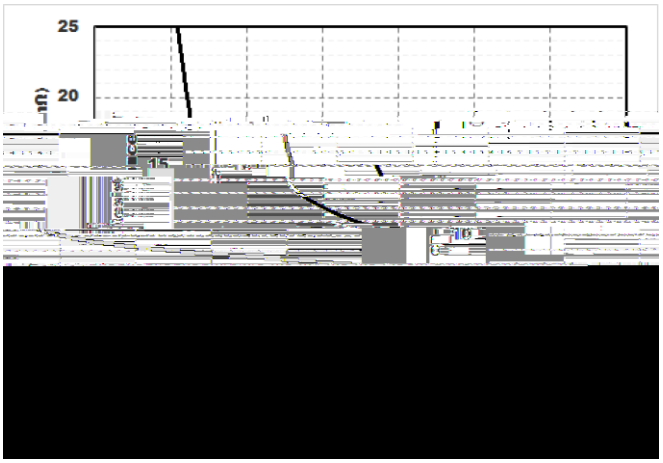


Figure5. **:** On-Resistance vs. Gate to Source Voltage

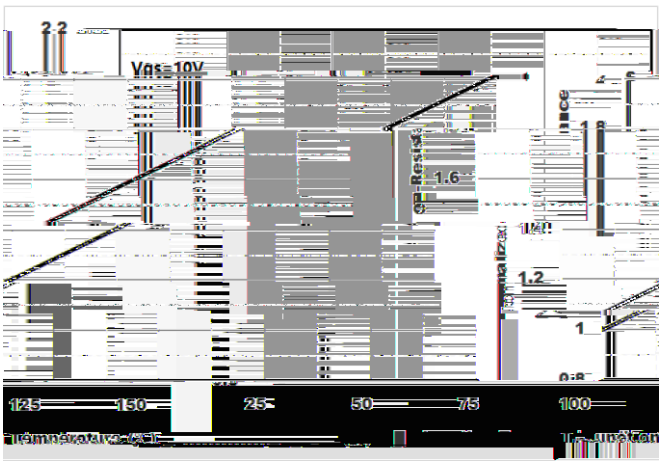


Figure6.Normalized On-Resistance

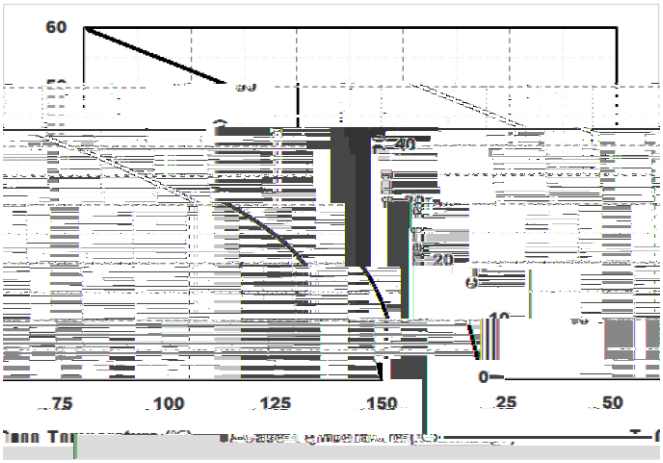


Figure7. Drain current

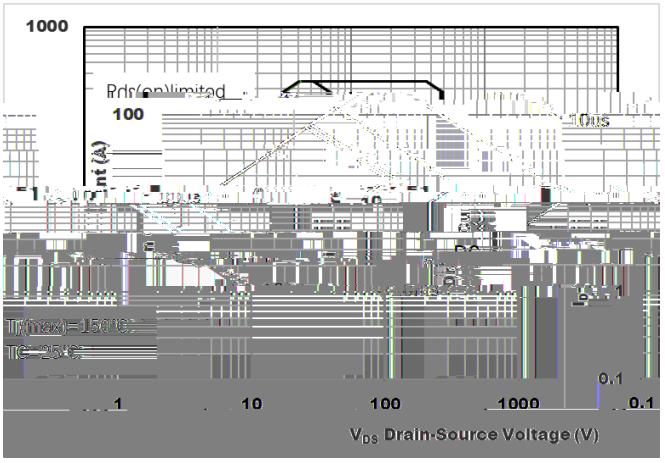


Figure8.Safe Operation Area

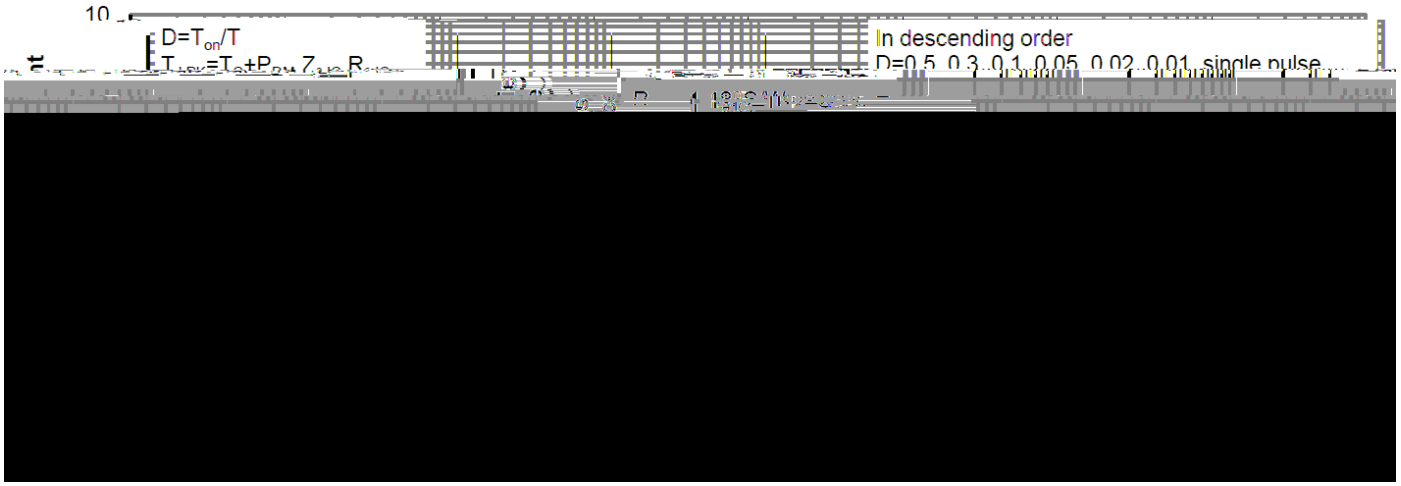
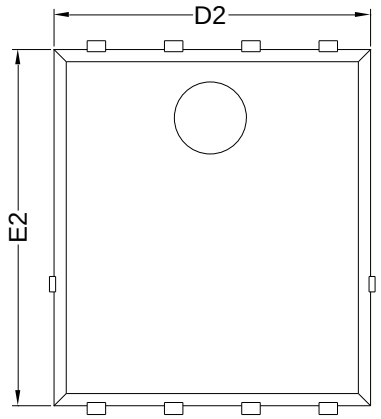
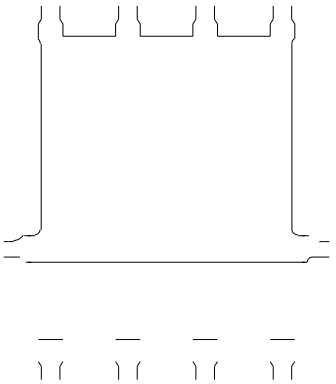


Figure9.Normalized Maximum Transient thermal impedance

PDFN5060-8L-B-1.1MM Package Information



Top View



Bottom View

Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254 REF	
E4		0.21 REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

Disclaimer

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