N-Channel Enhancement Mode Field Effect Transistor

Product Summary

ŏ V_{DS}	40V
ŏ I_D	50A
ŏ $R_{DS(ON)}$(at V_{GS}=10V)	4.5mq
ŏ $R_{DS(ON)}$(at V_{GS}=4.5V)	6mq
ŏ 100% EAS Tested	

General Description

ŏ Trench Power LV MOSFET technology
ŏ Excellent package for heat dissipation
ŏ High density cell design for low $R_{DS(ON)}$

Applications

ŏ High current load applications
ŏ Load switching
ŏ Hard switched and high frequency circuits
ŏ Uninterruptible power supply

ý **Absolute Maximum Ratings** (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25	I_D	12	A
	T_A=100		7.5	
	T_C=25		50	
	T_C =100		31	
[redacted]		I_{DM}	200	A
[redacted]				

ý **Electrical Characteristics** (T_J=25   unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units

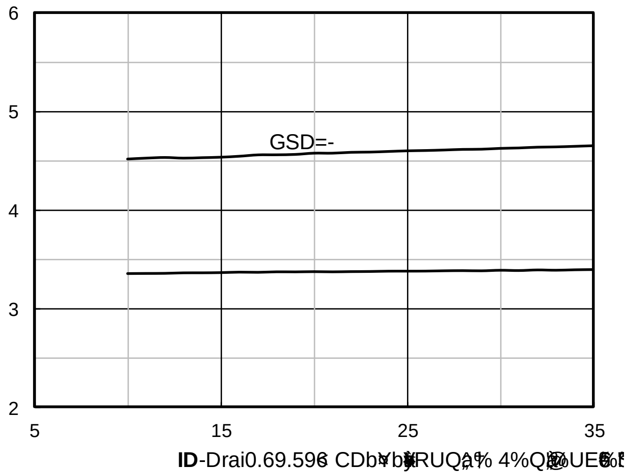


Figure 7. RDS(on) VS Drain Current

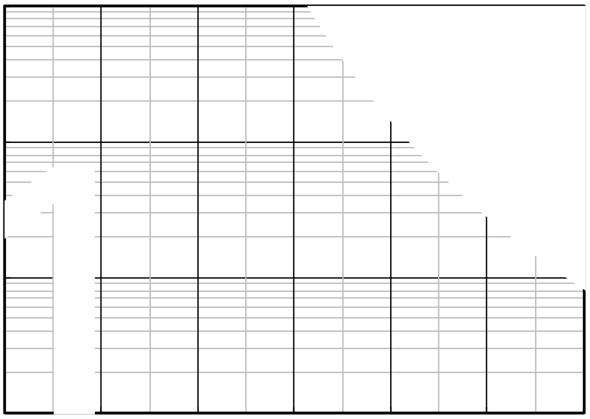
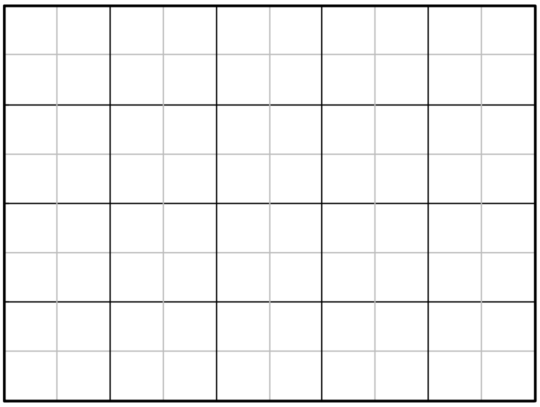
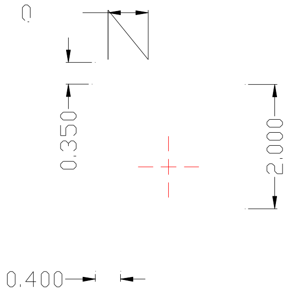


Figure 8. Forward characteristics of reverse diode



√ DFN3333-8L Package information



Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.10mm.
3.The pad layout is for reference purposes only.