RECOMMEND
YJT1D3G04HQ
FOR NEW DESIGN

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	40V
I_D	225A
$R_{DS(ON)}$(at V_{GS}=10V)	1.2m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free
-Q101 qualified

Applications

High power inverter system
Uninterruptible power supply
LCDM appliances

Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25	I_D	25	A
	T_A=100		17.8	
	T_C=25		225	
	T_C =100		159	
Pulsed Drain Current [A]		I_{DM}	400	A
Avalanche energy [B]		EAS	1441	mJ
Total Power Dissipation [C]	T_A=25	P_D	2	W
	T_A=100		1	
	T_C=25		166	
	T_C =100		8	

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D	40	-	[redacted]	

Typical Electrical and Thermal Characteristics Diagrams

Figure

Fe

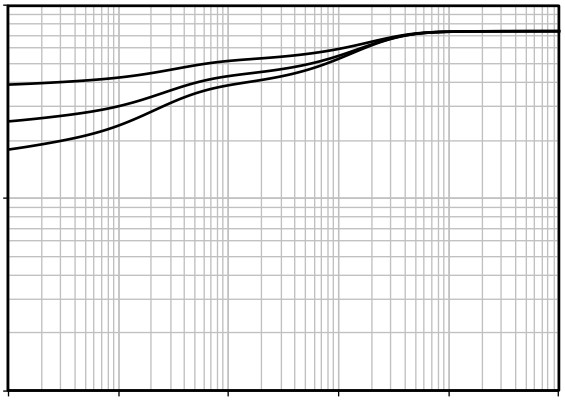

Figure 13. Maximum Transient Thermal Impedance

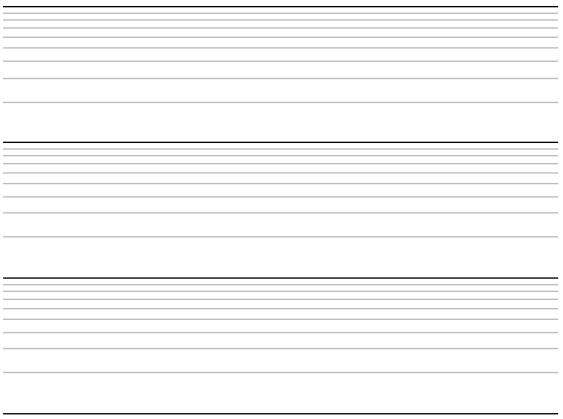

Figure 14. Safe Operation Area

TOLL Package information

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.2	2.3	2.4
A1	1.7	1.8	1.9
b	0.7	0.8	0.9
b1	9.7	9.8	9.9
b2	1.1	1.2	1.3
c	0.4	0.5	0.6
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.2	3.3	3.4
D3	4.45	4.55	4.65
E	9.8	9.9	10
E1	8	8.1	8.2
e	1.2 BSC		
H	11.58	11.68	11.78
H1	6.95 BSC		
i	0.1 REF		
j	0.46 REF		
L	1.5	1.6	1.7
L1	0.6	0.7	0.8
L2	0.5	0.6	0.7
L3	0.3	0.4	0.5
Q	8 REF		
R	3.0	3.1	3.2

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.03mm.
3.The pad layout is for reference purposes only.

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