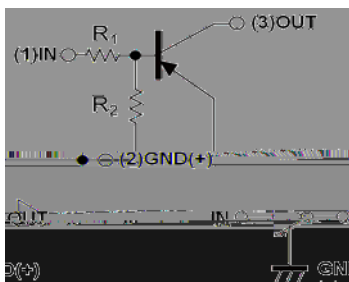
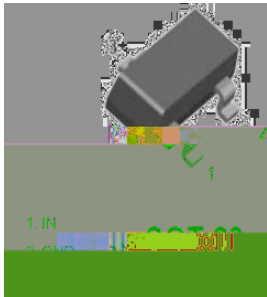




PNP Digital Transistors (Built-in Resistors)



Features

- Moisture sensitivity level 1
- Halogen free and RoHS compliant
- Surface mount package ideally suited for automatic insertion

Application

- Signal amplification
- Switching circuit

Mechanical data

- Package** SOT-23
- Terminals** Tin plated leads, solderable per J-STD-002 and JESD22-B102

Maximum Ratings ($T_a=25$ Unless otherwise specified)

Item	Symbol	Unit	Conditions	Value
Device marking code				13
Supply voltage	V_{CC}	V		-50
Input voltage	V_{IN}	V		-30 to +10
Output current	I_o	mA		-100
Power dissipation	P_D	mW		200
Junction temperature	T_J			-55 to +150
Storage temperature	T_{STG}			-55 to +150



DTA143ECA

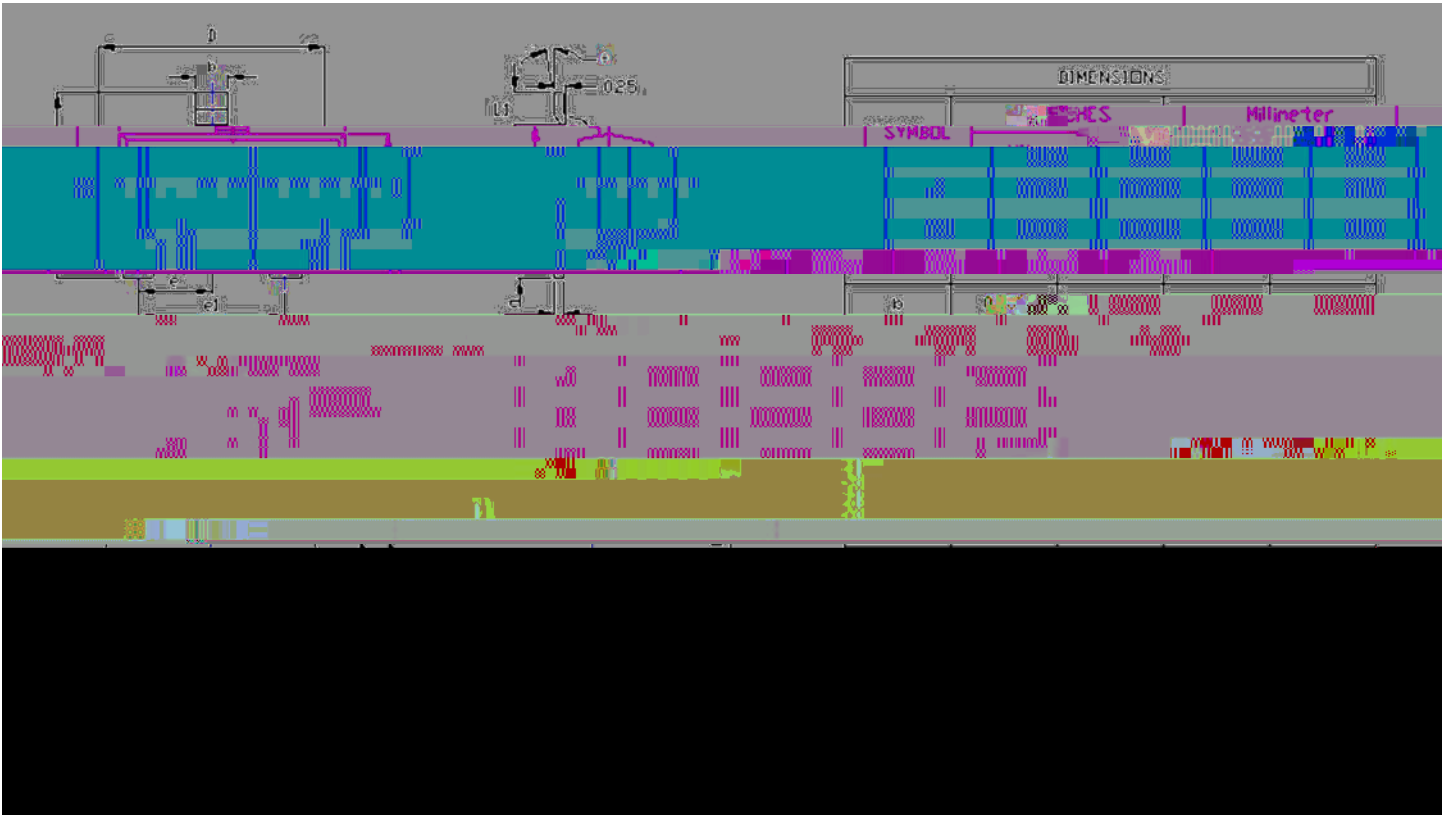
RoHS
COMPLIANT

Electrical Characteristics (T_a=25 Unless otherwise specified)

Item	Symbol	Unit	Conditions	Min	Typ	Max
Input voltage	V _{I(off)}	V	V _{CC} =-5V, I _O =-100uA	-0.5		
	V _{I(on)}	V	V _O =-0.3V, I _O =-20mA			-3.0
Output voltage	V _{O(on)}	V	I _O / I _I = -10mA / -0.5 mA			-0.3
Input current	I _I	mA	V _I =-5V			-1.8
Output current	I _{O(off)}	uA	V _{CC} =-50V, V _I =0			-0.5
DC current gain	G _I					



Outline Dimensions



Note:

1. All dimensions are in millimeters (mm) unless otherwise specified.

所有尺寸均以毫米(mm)为单位,除非另有规定。

4. All dimensions shown are exclusive of burrs and gate residues. Burrs and gate vestiges shall not exceed 0.15 mm in maximum.

所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的最大尺寸不得超过0.15mm。

5. Dimension b does not include the protrusion of the central rib on one side.

尺寸b不包括单边最大0.100mm的中筋凸出部分。

6. Dimension c is the external limit dimension of the package, excluding the mold flash, internal lead flash, protrusion and glue burr, but including the maximum offset of the package.

7. Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.

成型后的引脚应在同一平面,且相邻引脚的平面度应在0.076mm以内(最大取值取为0.100mm)。

8. ★ It is the key size.

[★ 标记为关键尺寸]



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