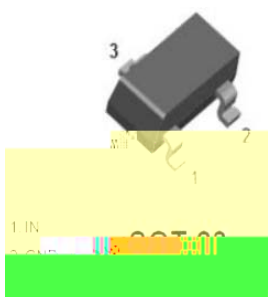
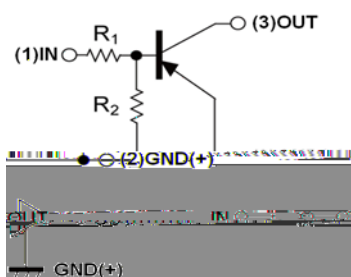


PNP Digital Transistors (Built-in Resistors)



Features

Application



Mechanical data Package Terminals

Maximum Ratings

Item	Symbol	Unit	Conditions	Value
Input voltage	V_i	V		- 2 0 to + 7
Output current	I_o	mA		-10 0
Power dissipation	P_D	mW		2 0 0
J unction temperature	$J T$			



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Electrical Characteristics

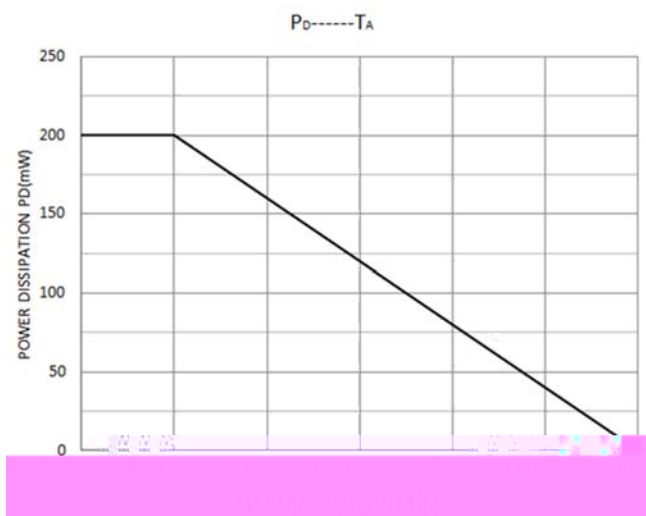
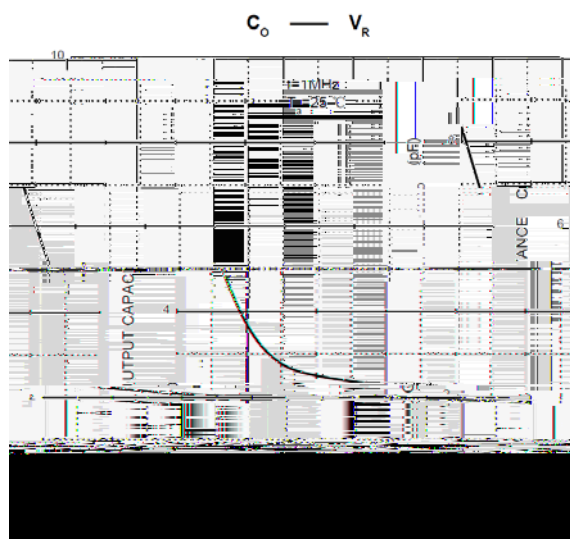
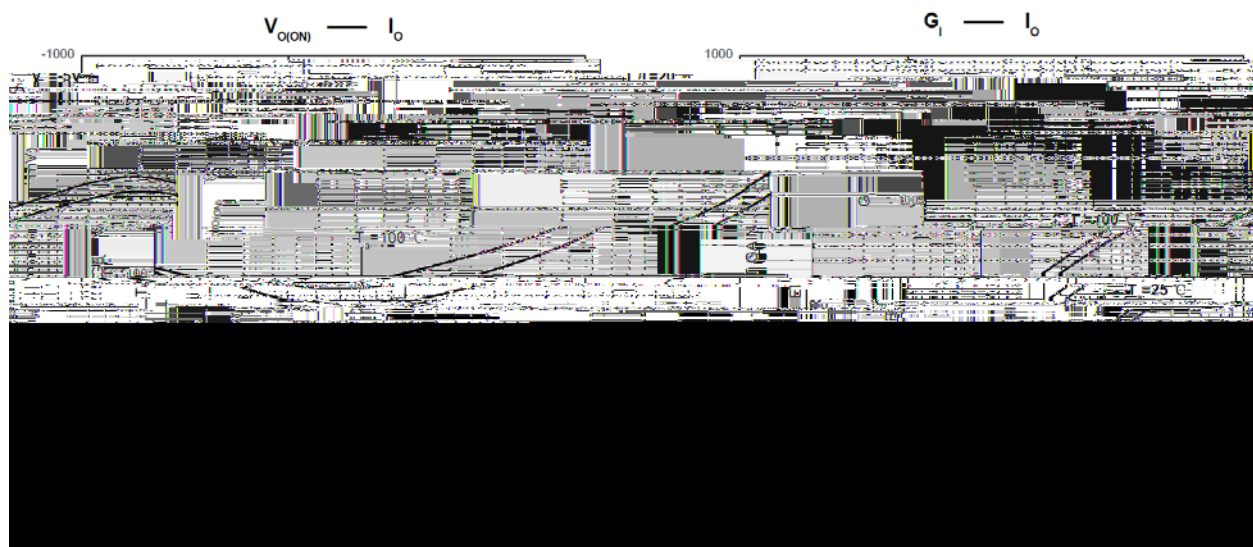
Item	Symbol	Unit	Conditions	Min	Typ
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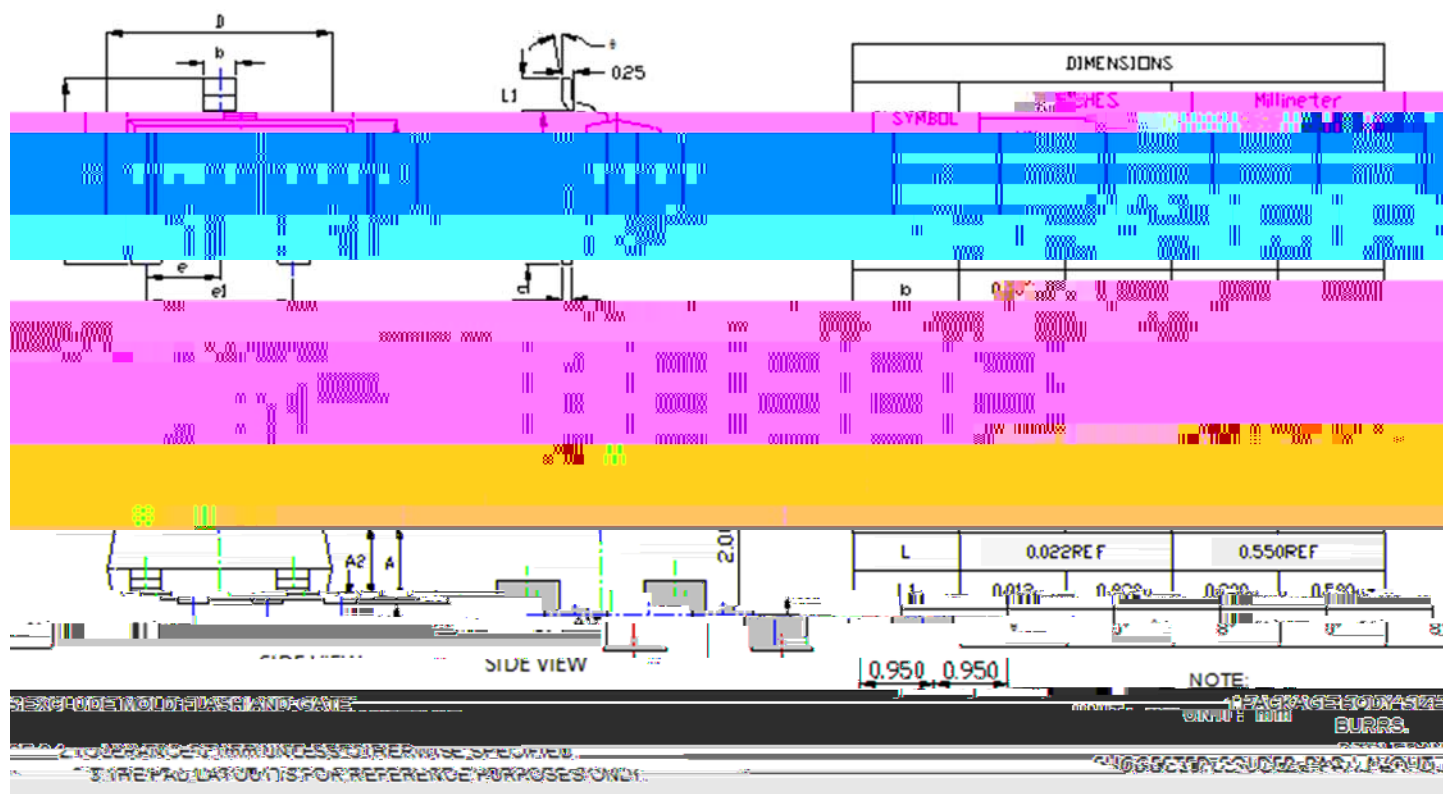
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Characteristics



Outline Dimensions



Note:

1. All dimensions are in millimeters (mm) unless otherwise specified.

1. All dimensions shown are exclusive of burrs and gate residues. Burrs and gate vestiges shall not exceed 0.15 mm in maximum.

1. 所有尺寸均不包括毛刺和胶体残留。毛刺和胶体残留不得超过0.15mm。

Dimension b does not include a maximum protrusion of max. 0.100 mm per side. [Dimension b does not include a maximum protrusion of max. 0.100 mm per side.]

尺寸b不包括单边最大0.100 mm的引脚凸出部分。 [尺寸b不包括单边最大0.100 mm的引脚凸出部分。]

Dimensions L and E are the external maximum dimensions; they do not include package mold mismatch.

[L和E是塑封体的外部极限尺寸；不包括包封溢料、内引线溢料、凸出部分以及胶体毛刺，但是包含了包封错位的最大尺寸。]

Dimensions L and E shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.

[L和E应在同一平面内，其平行度最大为0.076mm。]

key_size. [key_size.]

[尺寸] [尺寸]

7. Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.

[成型引脚应在同一平面内，其平行度最大为0.076mm。]

8. ★ It is the key size.

[★ 标记为关键尺寸]



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Disclaimer
